IN THE CLAIMS:

Please amend the claims as follows:

1-20. Canceled.

21. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a read request:

a first microinstruction causes data to be read from all ways in the cache, and

if the read request hits the cache, a second microinstruction causes data to be read from a target way, all other ways being disabled during performance of the second microinstruction.

22. (Currently amended) The cache control method of claim 21, further comprising:

reading data from a victim allocation unit during performance of the first microinstruction and

disabling the victim allocation unit during performance of the second microinstruction.

23. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a data replacement request, a microinstruction causes data to be written to a tag field and data field in a single way, all other ways being disabled during performance of the microinstruction.

24. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a write request made pursuant to an eviction from a higher level cache:

a first microinstruction causes data to be read from tag fields from all ways of the cache, all other fields in the ways being disabled during performance of the first microinstruction, and

if the data request hits the cache, a second microinstruction may energize a tag field and data field of a matching way, all other ways being disabled during performance of the second instruction.

25. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a cache writeback invalidate instruction:

a first microinstruction causes a victim way to be enabled, all other ways being disabled during performance of the first microinstruction, and

if an addressed cache entry in the victim way stores valid data, a second microinstruction causes data to be written in a state field of the cache entry, all other ways being disabled during performance of the second microinstruction.

26. (Currently amended) The cache control method of claim 24, wherein all other fields of the cache entry are disabled during performance of the second microinstruction.

27. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a cache invalidate request, a microinstruction causes data to be written in a state field of an addressed cache entry in a target way, all other ways being disabled during performance of the microinstruction.

28. (Currently amended) The cache control method of claim 27, wherein all other fields of the cache entry are disabled during performance of the microinstruction.

29. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a write pursuant to a read-for-ownership request issued by higher level cache, a microinstruction causes data to be written in a tag field and a state field of an addressed cache entry in a target way, all other ways being disabled during performance of the microinstruction.

30. (Currently amended) The cache control method of claim 29, wherein all other fields of the addressed cache entry are disabled during performance of the microinstruction.

31. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a snoop probe, a microinstruction causes data to be read from tag fields and state fields through all ways in the cache, all other fields throughout the cache being disabled during performance of the microinstruction.

32. (Currently amended) The cache control method of claim 31, wherein, if the data request hits the cache and state data of a matching cache entry represents exclusive state, a second microinstruction causes data to be written to a state field of the matching cache entry, all other ways are disabled during performance of the second microinstruction.

33. (Currently amended) The cache control method of claim 31, wherein, if the data request hits the cache and the snoop probe is not a Go-to-Shared snoop, a second microinstruction causes data to be written to a state field of the matching cache entry, all other ways are disabled during performance of the second microinstruction.

34. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a snoop confirm request with associated data, a microinstruction causes data to be read from a data field of a cache entry in a single way and data to be written

to a state field of the cache entry, all other ways are disabled during performance of the microinstruction.

35. (Currently amended) A cache control method comprising:

in response to a data request, generating at least one microinstruction within a cache,

disabling predetermined portions of the cache based on the microinstruction, wherein, when the data request is a snoop confirm request with no associated data, a microinstruction causes data to be written to a state field of a cache entry in a single way, all other ways are disabled during performance of the microinstruction.

36-37. Canceled.